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EXAMINER	
DICKEY, THOMAS L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,764	YONEMARU, MASASHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' "Summary of the Invention" section in their appeal brief points out a deficiency in the Action mailed 6/22/07.

The summary section of Applicants' Appeal brief describes an invention different from the invention rejected in the Action mailed 6/22/07. The differences appear to stem from an ambiguity (discussed below) in the claim language. The invention rejected 6/22/07 might reasonably be the claimed invention. Therefor the rejection mailed 6/22/07 stands. The invention Applicants describe in their Appeal brief might reasonably be the claimed invention. This invention has been searched, its closest art identified, and a second rejection, based on this second reasonable interpretation of the ambiguous language, has been added.

This action is responsive to substantial amendments to the claims filed 10/17/2006 (amendments made in response to a first action on the merits) and is made final for that reason.

Claim Objections

2. Claims 1, 6, and 8 are objected to because of the following informalities:

In claim 1 lines 10-18, the language:

> the second cell functions as a driver circuit for driving the logic operation circuit and a data retaining circuit for retaining data output by the logic operation circuit

might reasonably mean (meaning "A"):

> the second cell functions as a driver circuit for driving the logic operation circuit and the second cell ALSO functions as a data retaining circuit for retaining data output by the logic operation circuit

Note that this language is an amended version of similar language presented in the claim set entered 7/5/05. A "marked up" version of the amended language would read:

> the second cell functions as ~~at least one of~~ a driver circuit for driving the logic operation circuit **and** ~~or~~ a data retaining circuit for retaining data output by the logic operation circuit

However, as the claim presently is written, one of skill in the art could also reasonably interpret this phrase as meaning (meaning "B"):

> the second cell functions as a driver circuit for driving a complex circuit, said complex circuit comprising:
>
> > the logic operation circuit and a data retaining circuit for retaining data output by the logic operation circuit

This language is not indefinite because it definitely has either meaning "A" or meaning "B." This language is merely ambiguous. It is noted that in their recent appeal brief, Applicants have summarized their invention according to meaning "B." At page 7 of their brief Applicants describe the invention as including "a data retaining circuit (e.g., see 3 in Fig. 4; pg. 15, lines 16-18; pg. 49, lines 4-5) for retaining data output by the logic operation circuit (e.g., see 2 in Fig. 4)" that is not part of the claimed "second cell (e.g., S2 in Fig. 1B)". On the other hand, in the last final rejection the Examiner rejected the claims assuming meaning "A" (second cell functions as a driver circuit for driving the logic operation circuit and the second cell ALSO functions as a data retaining circuit). In the current final rejection the claims have been rejected twice, first assuming meaning "A" and next assuming meaning "B."

Although the language is merely ambiguous and not indefinite, Applicants are nonetheless required to eliminate the ambiguity. Applicants may rewrite this phrase to clearly express meaning "A," to clearly express meaning "B," or to clearly express a claim that can be met by either meeting meaning "A" or by meeting meaning "B." However, Applicants must clearly state their meaning.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by ROBINSON ET AL. (20050182809).

Robinson et al. discloses a semiconductor integrated circuit, comprising a first cell 62 comprising a plurality of transistors; a second cell 66 comprising a PMOS transistor section 72-74, the PMOS transistor section 72-74 comprising a first PMOS transistor 72 and a second PMOS transistor 74 connected to the first PMOS transistor 72 in series,

and an NMOS transistor section 76-78, the NMOS transistor section 76-78 comprising a first NMOS transistor 76 and a second NMOS transistor 78 connected to the first NMOS transistor 76 in series, wherein a predetermined scheme is used to connect between the first cell 62 and the second cell 66, between the plurality of transistors in the first cell 62, and between the PMOS transistor section 72-74 and the NMOS transistor section 76-78 in the second cell 66, wherein the first cell 62 functions as a logic operation (barrel-shifting) circuit for outputting data; and the second cell 66 functions as a driver circuit (by way of feedback or "pull-up" transistor 79) for driving the logic operation circuit and the second cell ALSO functions as a data retaining circuit ("dynamic latch," note paragraphs 0050-0052) for retaining data output by the logic operation (barrel-shifting) circuit, and wherein the first PMOS transistor 72, the second PMOS transistor 74, the first NMOS transistor 76, and the second NMOS transistor 78 each comprise a gate, a source, and a drain; a first source voltage is applied to the source of the first PMOS transistor 72; a second source voltage is applied to the source of the first NMOS transistor 76; one of the gate of the first PMOS transistor 72 and the gate of the second PMOS transistor 74 is connected to an input terminal IN, an input signal being input to the input terminal IN, and the other is connected to a first gate control signal input terminal ϕ(clock signal), a first gate control signal being input to the first gate control signal input terminal ϕ; one of the gate of the first NMOS transistor 76 and the gate of the second NMOS transistor 78 is connected to the input terminal IN, and the other is

connected to a second gate control signal input terminal ϕ-BAR (inverse clock signal), a second gate control signal being input to the second gate control signal input terminal ϕ-BAR; and the drain of the second PMOS transistor 74 and the drain of the second NMOS transistor 78 are connected to an output terminal OUT. Note figures 8, 9, and paragraphs 0049-0055 of Robinson et al.

B. Claims 1, 6, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by ROBINSON ET AL. (20050182809).

Kajigaya et al. discloses a semiconductor integrated circuit comprising a first cell CDCR comprising a plurality of transistors including a PMOS transistor and an NMOS transistor; a second cell CADB comprising a PMOS transistor section, the PMOS transistor section comprising a first PMOS transistor Q1 and a second PMOS transistor Q2 connected to the first PMOS transistor Q1 in series, and an NMOS transistor section, the NMOS transistor section comprising a first NMOS transistor Q11 and a second NMOS transistor Q12 connected to the first NMOS transistor Q11 in series, wherein a predetermined scheme is used to connect between the first cell CDCR and the second cell CADB, between the plurality of transistors in the first cell CDCR, and between the PMOS transistor section and the NMOS transistor section in the second cell CADB, wherein the first cell CDCR functions as a logic operation circuit (note column 4 lines 38-42) for outputting data; and the second cell CADB functions as a driver circuit (note column 4 lines 46-55) for driving a circuit comprising the logic

operation circuit CDCR and a data retaining circuit CSW for retaining data (note, again, column 4 lines 38-42) output by the logic operation circuit CDCR; the first PMOS transistor Q1, the second PMOS transistor Q2, the first NMOS transistor Q11, and the second NMOS transistor Q12 each comprise a gate, a source, and a drain; a first source voltage may be applied via bit line Vcc to the source of the first PMOS transistor Q1; a second source voltage may be applied via another bit line (indicated in figure 2 with an inverted triangle) to the source of the first NMOS transistor Q11; one of the gate of the first PMOS transistor Q1 and the gate of the second PMOS transistor Q2 may be connected via a word line to an input terminal tm, an input signal being input to the input terminal tm of second PMOS transistor Q2, and the other is connected to a first gate control signal input terminal tm, a first gate control signal being input to the first gate control signal input terminal tm; one of the gate of the first NMOS transistor Q11 and the gate of the second NMOS transistor Q12 is connected to the input terminal tm PRT, and the other is connected to a second gate control signal input terminal A0, a second gate control signal being input to the second gate control signal input terminal A0; and the drain of the second PMOS transistor Q2 and the drain of the second NMOS transistor Q12 are connected to an output terminal ay0. Note figures 1, 2, 4, column 3 lines 5-68, column 4 lines 1-46, and column 8 lines 6-62 of Kajigaya et al.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over ROBINSON ET AL. (20050182809) in view of Murakami (5,457,723).

Robinson et al. discloses a semiconductor integrated circuit having every limitation of claim 6 except the limitation that the first cell must include a P-MOS transistor and an N-MOS transistor. Note figures 8, 9, and paragraphs 0049-0055 of Robinson et al.

However, Murakami discloses a semiconductor integrated circuit with a first cell identical in form and function (barrel shifter) to Robinson et al.'s (barrel shifter) first cell, except Murakami's first cell barrel shifter includes a P-MOS transistor P31 and an N-MOS transistor N31. Note figures 4 and 5 and column 4 lines 16-22 of Murakami. Murakami explains that "the barrel shifter having the circuit of CMOS structure described at column 4 lines 16-22 and shown in FIG. 4 and FIG. 5 requires no circuit for loading the initial data and has such an ideal advantage of reducing electric consumption as that it is operable from high frequency to clock stop condition. This is extremely advantageous for so-called lap top type or palm top type microcomputers which operate primarily from a battery." It would therefore have been obvious to a

person having skill in the art to modify Robinson et al.'s semiconductor integrated circuit by including the P-MOS and N-MOS transistors in the first cell, such as taught by Murakami), in order to avoid requiring a circuit for loading the initial data to thus reduce current consumption as would prove advantageous in battery operation.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 6, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment, filed 10/17/2006, necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826